X 1210 Mono Disk Drive

Volume 5 - Electronics

(preliminary
information)

Write - Read- procedures and

Power supply in X 1210

Aut: Th. G. Schoof

Reg. no. CNR.I.420.1100.007

Date: 3 aug. 1971

CONTENTS

1. S U M M A R Y

In the X 1210 Mono Disk Drive a 14" magnetic disk is rotating with a speed of 800 R.P.M. Two selectable floating tunnel-erase-heads can write and read on both sides over an area of 200 tracks.
Information can be stored in a frequency-doubling code with a density of 2200 b.p.i. and a bitrate of 833 kHz.
The magnetic writing - and erasing - fields are generated with a write - erase - amplifier connected as a voltage source.
The read channel is build up with a lineair preamplifier, a phasecorrecting network with limiter, and a sampling read-recovery with a flywheel - oscillator.
The AC - and DC - supply can be derived from the power supply unit XMX 1407.

P R E F A C E

This report was written as a syllabus supporting a course for field engineers servicing the X 1210 Mono-Disk-Drive. The present subject deals with those parts of the system needed for the input and recovery of information only. (Write channel and read channel respectively).
Furthermore is intended to provide enough view on the function of the system and the associated circuits that independent servicing, maintenance and adjustments can be made.
For clearness and better understanding some attention is paid to common recording technic. In addition, chapter 6 illustrates the power supplies.

3. G E N E R A L

The X 1210 is a memory designed with one rotating magnetic disk on both sides of which information can be stored and restored by means of two registration heads. The heads are of the "floating" type, they fly on a "height" of 2 /um over the surfaces of the disk.The twin headset can be moved in radical direction so the entire disk surfaces can be reached. A schematic structure is given in fig. 1

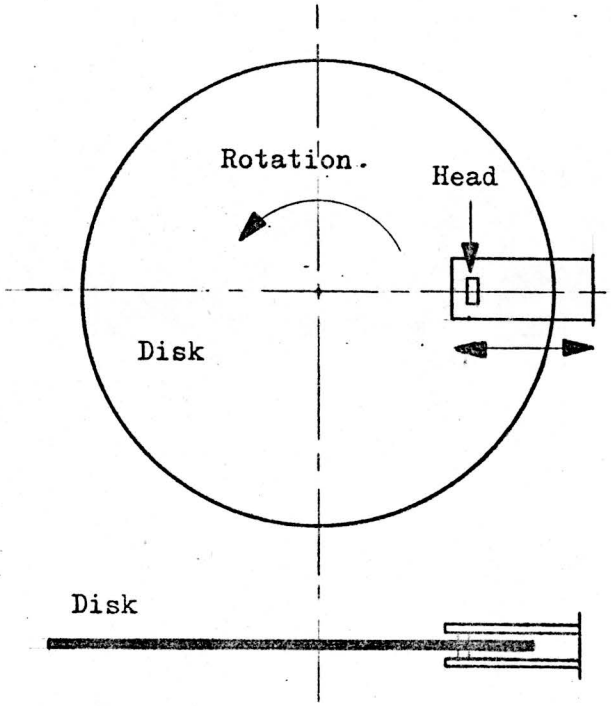


Fig. 1

3.1 THE DISK

The disk is a 14 inch standard type as widely used in other kinds of memories. The substrate is made of an aluminium aloy, coated with 2 µm of ironoxide (FeO). The remanence in the hysteresis curve shown in fig. 2 is the main property used to store information as reversals in magnetic polarity. The reversals are written in 200 concentric tracks each 140 µm wide. The smallest diameter is 230 mm, the largest 330 mm, corresponding with a trackvelocity of 9,6 m/sec and 13,8 m/sec respectively.

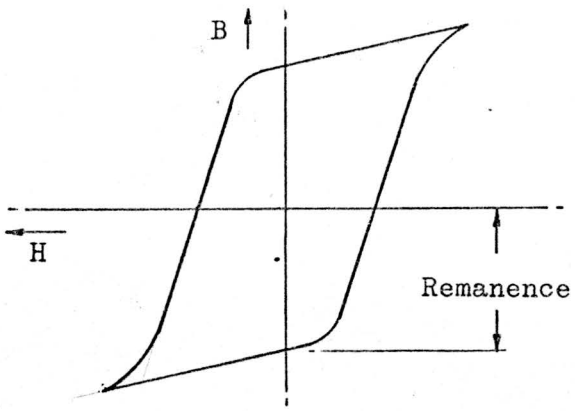


Fig. 2

3.2 THE HEAD

During writing a magnetic field is generated with the write/read-head thus saturating the magnetic coating on the disk over a trackwidth of 210 µm. By changing the the polarity of this field the fluxreversals can be written. By means of a build-in erasing structure the trackwidth is reduced to 140 µm and the vicinity of the track is cleaned from previously written information . (Tunnel erase). During reading the passage of the fluxreversals generates voltages with some millivolts of amplitude in the same head.
Fig. 3 gives a schematic layout.

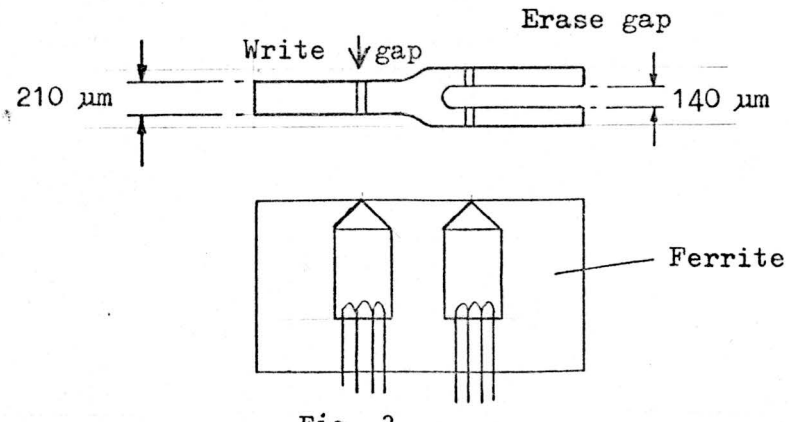


Fig. 3

3.2.1 MECHANICAL CONSTRUCTION

Fig. 5 gives an outline of the composition of the magnetic headcore and the attachment to the floatingshoe. To meet the close tolerances the write/read-head and the erasehead, in fact two different heads, are made out of one piece of ferrite. To prevent magnetic coupling which should lead to crosstalk, the ferrite between the two coils is partly replaced by a nonmagnetic white ceramic. The head with floatingshoe is springmounted in the headarm and pneumatic loaded with a force of 160 gr.

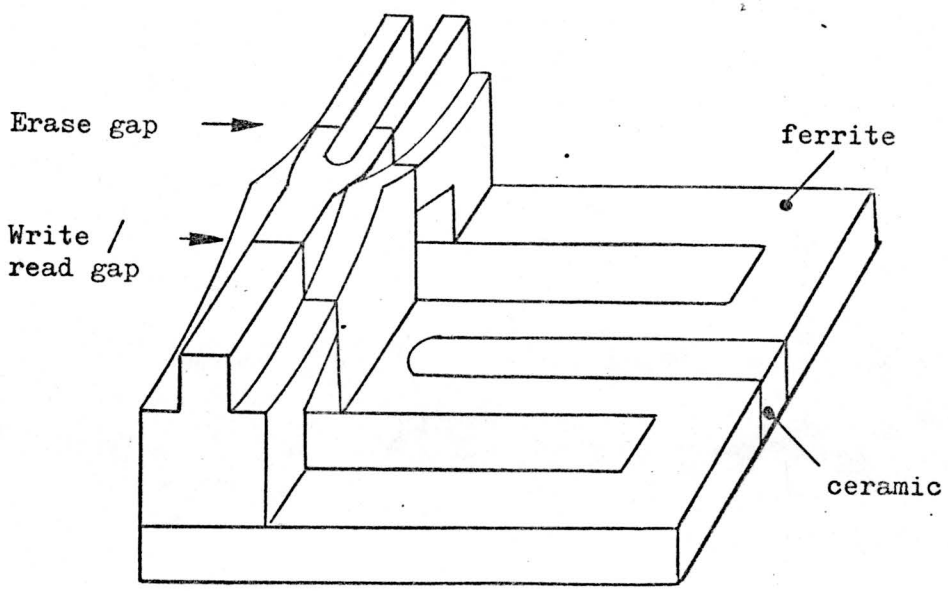
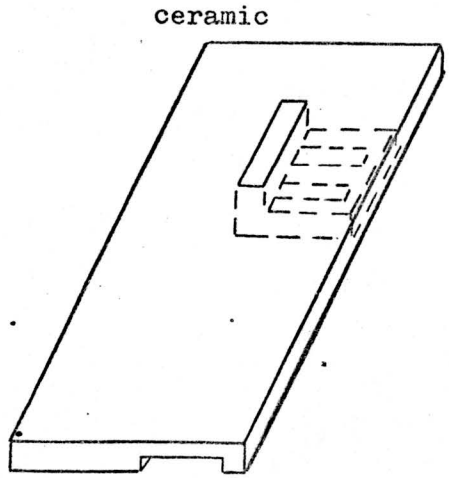


Fig. 4



3.2.2 ELECTRICAL CONSTRUCTION

To generate the writefield two coils L1 and L2 with 54 windings each are laid around one outer leg of the magnetic core. (Selfinduction 2 x 60/uH, wire diameter 40/um.) The required fieldstrength is reached with a current of 25 mA through L1 or L2, depending on the desired fielddirection. A current of 30 mA through the erasecoil L3 provides the erasefield. L3 is wound around the other outer coreleg with 38 windings of 50/um - wire. (Selfinduction 30/uH). The three coils have a common return connection also used for headselection. See fig. 5.

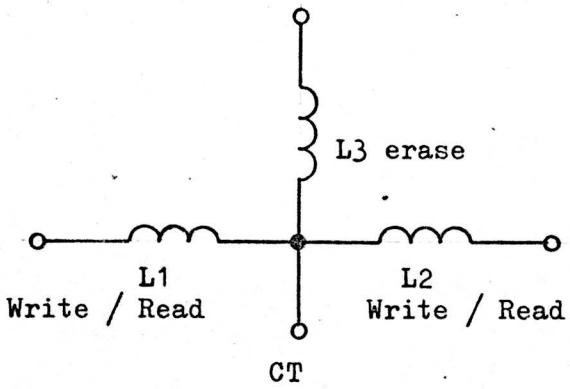


Fig. 5

3.3 WRITING

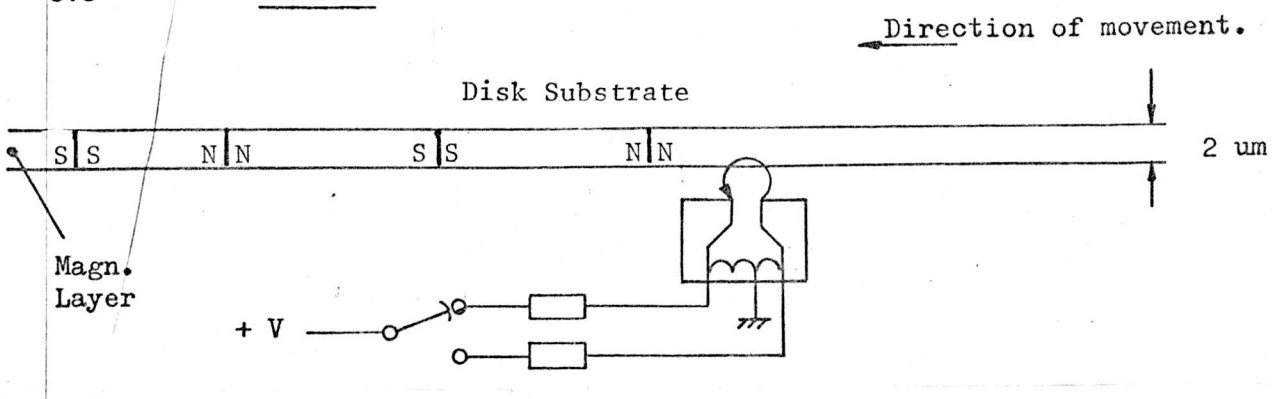


Fig. 6

After the magnetic material of the disk has passed the gap of the writing head the fluxreversals remain on the disk as shown in fig. 6. Every reversal represents an information bit, the interpretation of which depends on the used code. In the X 1210 the self-clocking frequency doubling FM-code is used. See fig. 7

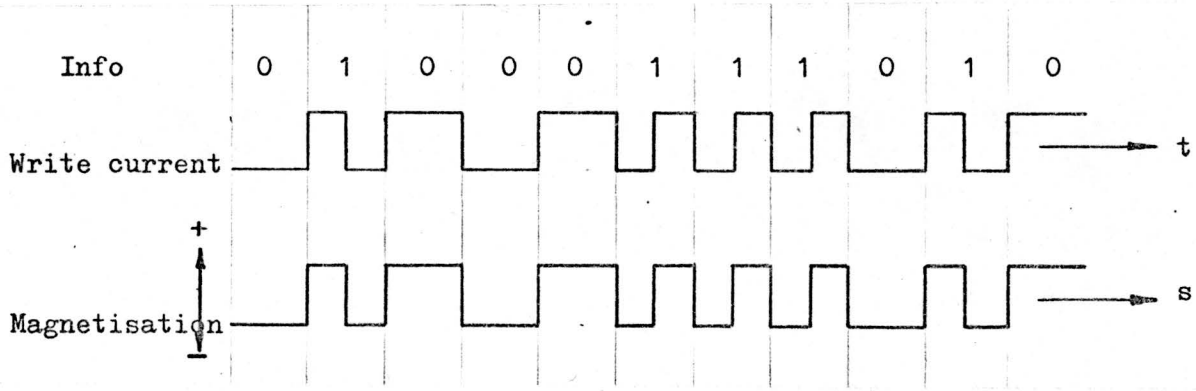
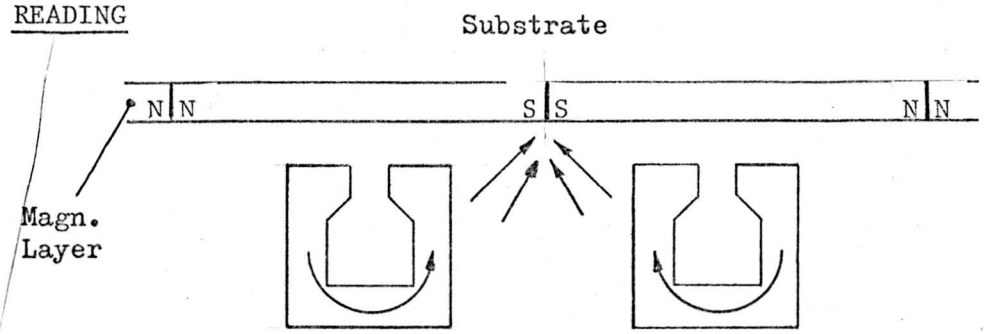


Fig. 7

As can be seen, for every one-bit a reversal is written, while to every bit an extra reversal is added for clock-information. This causes two fundamental frequencies of 0,417 Mc/s and 0,833 Mc/s. With a trackvelocity of 9,6 m/sec the minimum distance between two reversals will be 5,76 um, according with a density of 4400 rev./inch. (2200 b.p.i.).

3.4 READING



Field lines
in flux reversal

Fig. 7

As a magnetic fluxreversal passes the gap of a reading head the direction of the fieldlines in the headcore will reverse. Fig.7. This generates a voltage in the headcoils proportional to $V = \frac{d\phi}{dt}$.

The pulseform agrees well with the mathematical formula $Y = \frac{1}{1+X^2}$ (fig. 8). The top of the pulseform represents the position of the magnetic reversal. It will be clear that adjacent read-pulses always have the opposite polarity. So in this way, when the information contains only zero's, the read voltage is almost sinusoïdal with a frequency of 0,417 Mc/s and in the case of only one's the frequency will be 0,833 Mc/s.

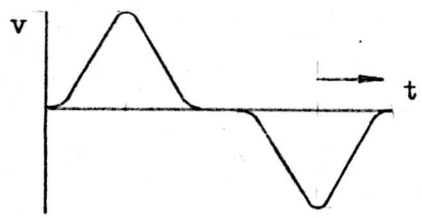


Fig. 8

In this case with high density, the follow up time of the pulses is so short that overlap (crowding) occurs. This causes a decrease of amplitude and a pattern dependent peakshift. (Fig. 9) With a variable bitconfiguration the latter in turn causes timejitter.

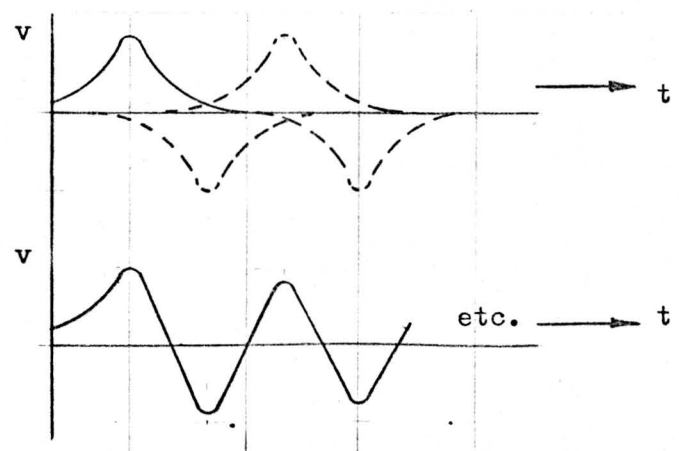


Fig. 9

The functions of the read channel is to restore the original write signal out of the small signals (0,25 mV - 2 mV) from the readhead. The deviations are mainly caused by the differentiating character of the write-read-process and the loose of harmonic components where is compensated for in the readamplifiers. The pattern dependent jitter is faced with the aid of a flywheel oscillator and a sampling system. See fig. 10.

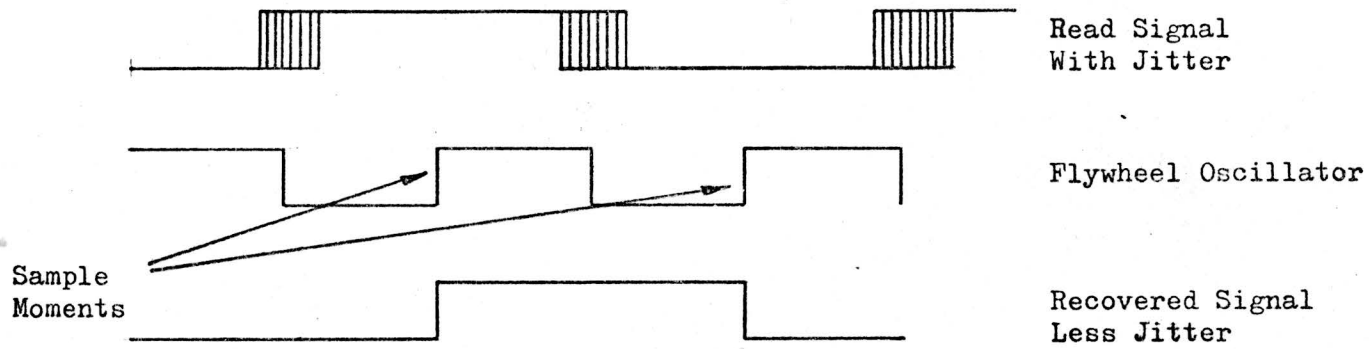


Fig. 10

The frequency of the flywheel oscillator can follow slow variations caused by rotation speed but cannot be disturbed by the fast variations that occurs between bits. In fig 11 all important signals are given in the correct timerelation.

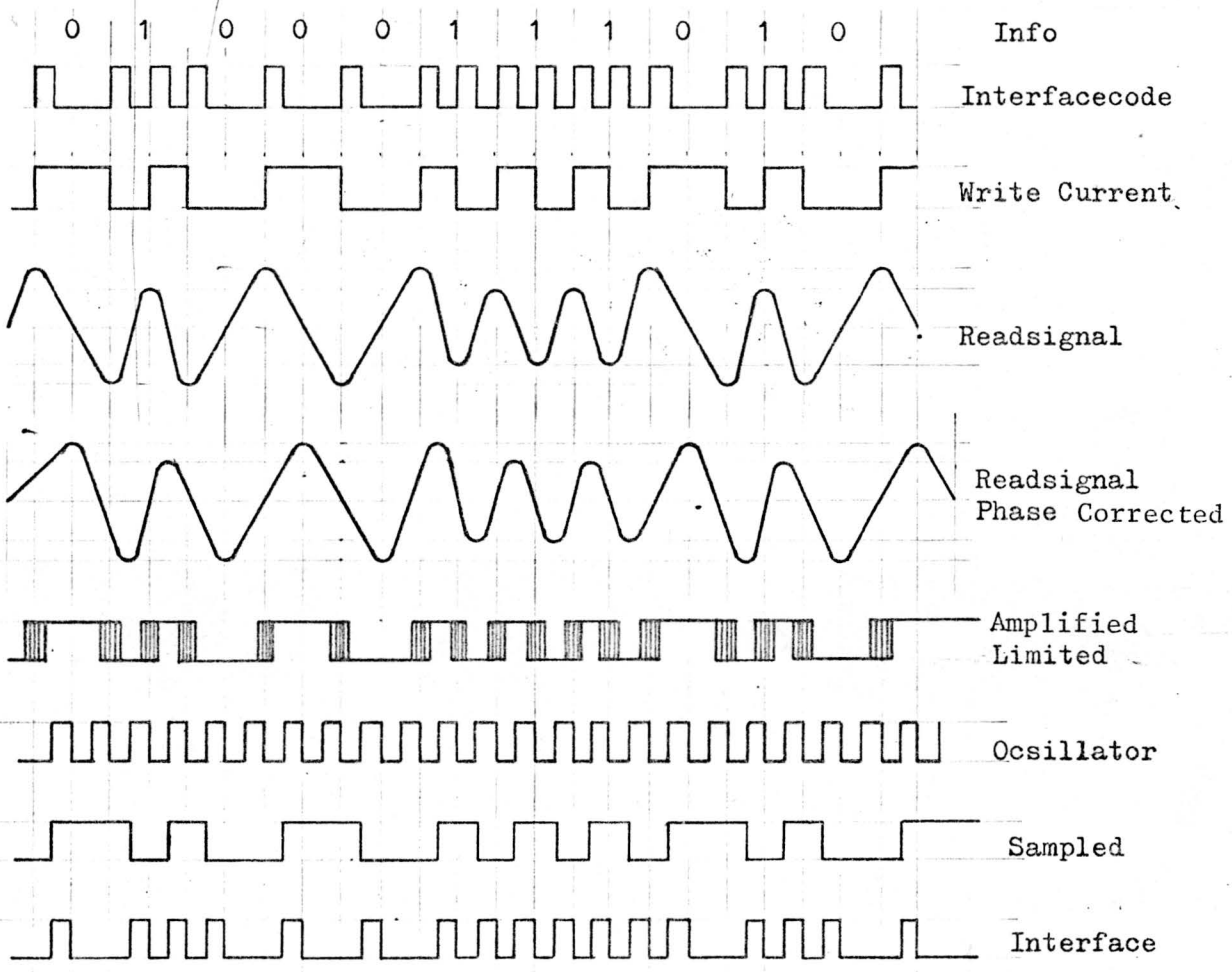


Fig. 11

4. REALISATION

In fig. 12 a blockdiagram of the complete write/read system in the X 1210 is drawn.

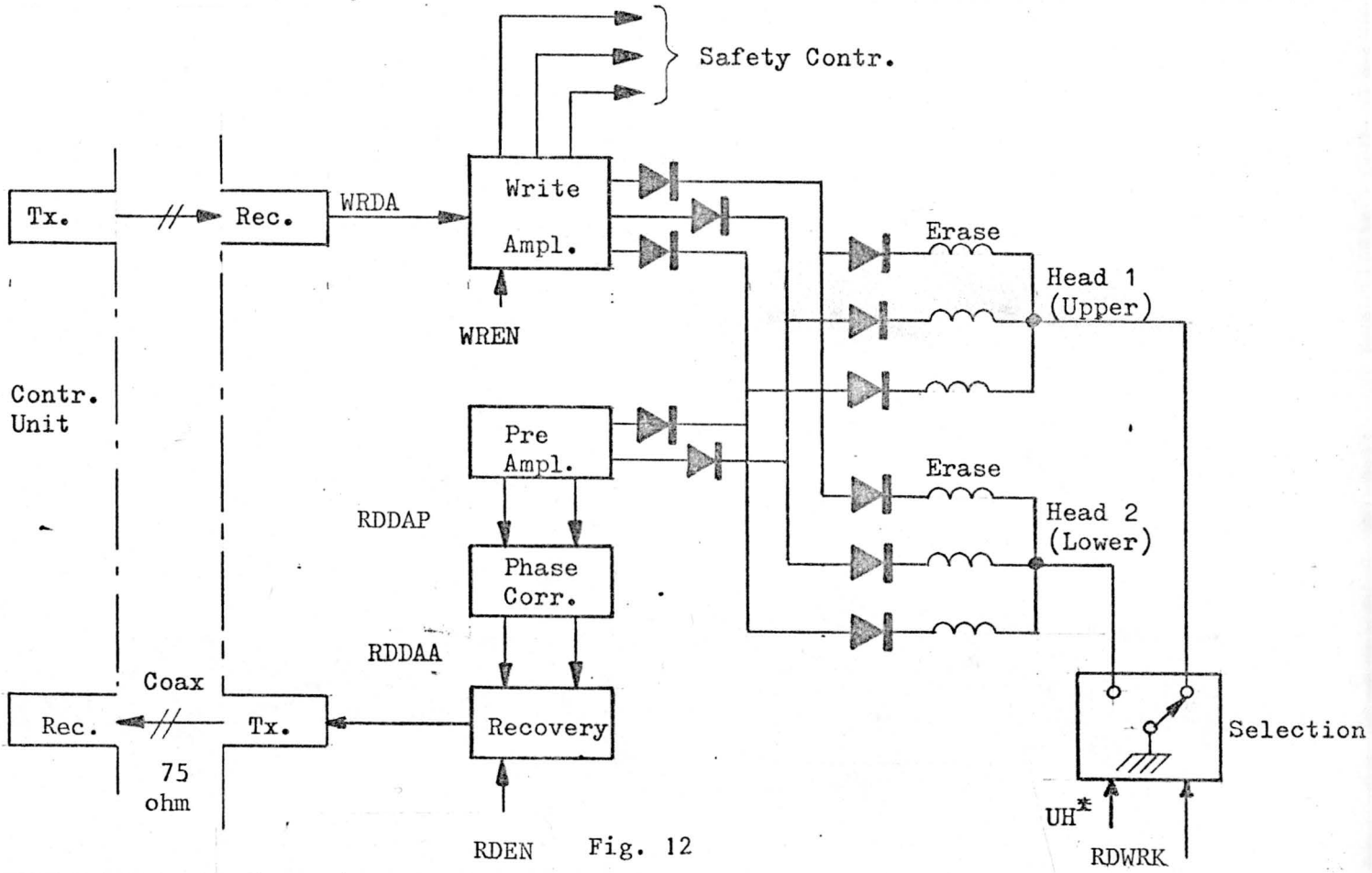


Fig. 12

In the following pragraphs the associated cards will be discussed briefly.

4.1 TRANSMITTER-RECEIVER (dwg. no. 5132 199 6110)

The cable transmitter and receiver circuits for the data signals are housed on card 12. Because the cable-length should be kept within 3 m (10 ft.) between control unit and X 1210, a simple connection with 75 ohm coax-cable and standard logical powernands could be used. (FJH 141 - SN744oN, TTL - dual nand powergate)

4.2 WRITE-ERASE-AMPL./SAFETY. (dwg. n° 5132 199 0110)

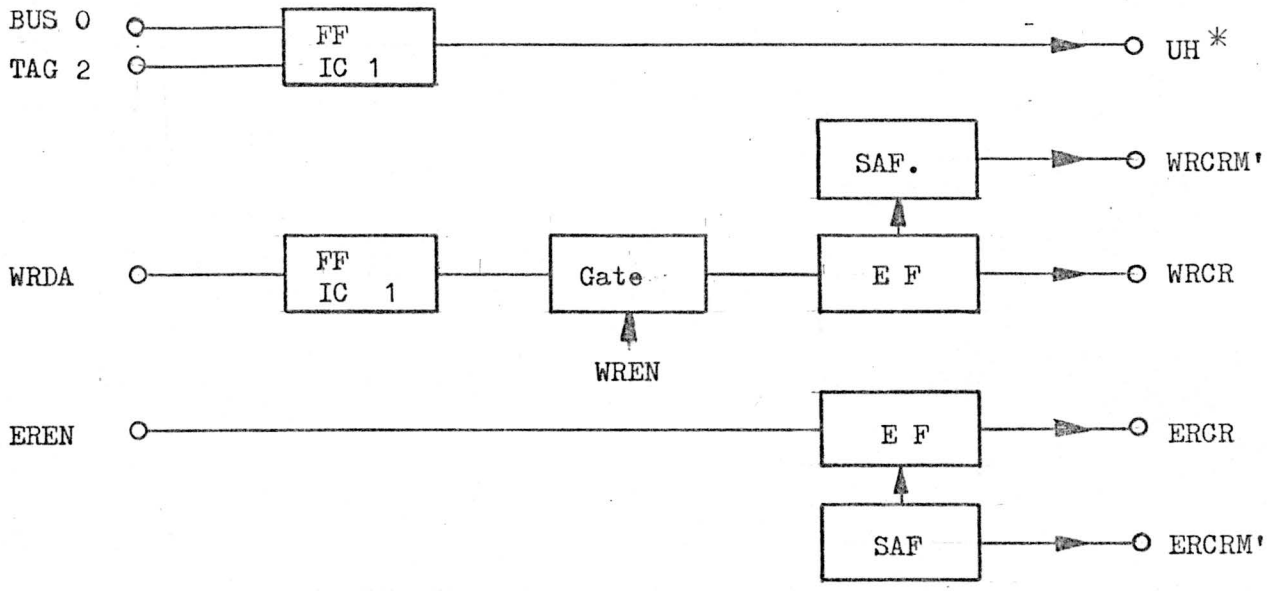


Fig. 13

The write - erase - amplifier/safety - card (Fig. 13) includes the circuits for generating and gating the write and erase currents. The flip-flop (FF) for head selections is build-in at the same card.

4.2.1 WRITE SECTION

The signal WRDA (write data) is fed from the cable receiver to one of the D-flip-flops (FF) in IC1. The cablecode is transferred to real FM-code that means that every pulse is transferred to a pulse-edge.
The signals from IC1 are coupled to the gate circuit TS 5-6-7-8 via the emitter followers (EF) TS 2-3.
The gate is activated by the signal WREN (write enable) thus preventing TS 4 from drawing current during writing.
From the collectors of Ts 5-7 pulses with an amplitude of approximately 24V are obtained driving the output-emitter followers TS 11-12. The output pulses and a couple of external resistors housed on the pre-amplifier determine the current through the head on 25 mA per half coil.
When TS 4 conducts (WREN ≙ "1") TS 5 and TS 6 as well as TS 7 and TS 8 draw enough current to keep both output collectors on zero volts and no write current can flow.

4.2.2 ERASE SECTION

In a similar way but without gating possibility, an erasecurrent of 30 mA is generated with TS 9 and TS 10.
In this case the resistors determining the current value are housed within the card (R 35-36-37).

4.2.3 SAFETY SECTION

For safety requiremtns after write data are presented, the current flow in the head is monitored with TS 13-14-15 and TS 16-17-18. The presence of current is checked at the collectors of TS 11-12. The capacitors C 9-10 with the associated resistors introduce a delay in the positive-going edges of 300 à400 n sec, a necessity for the safety system. (see fig. 14).

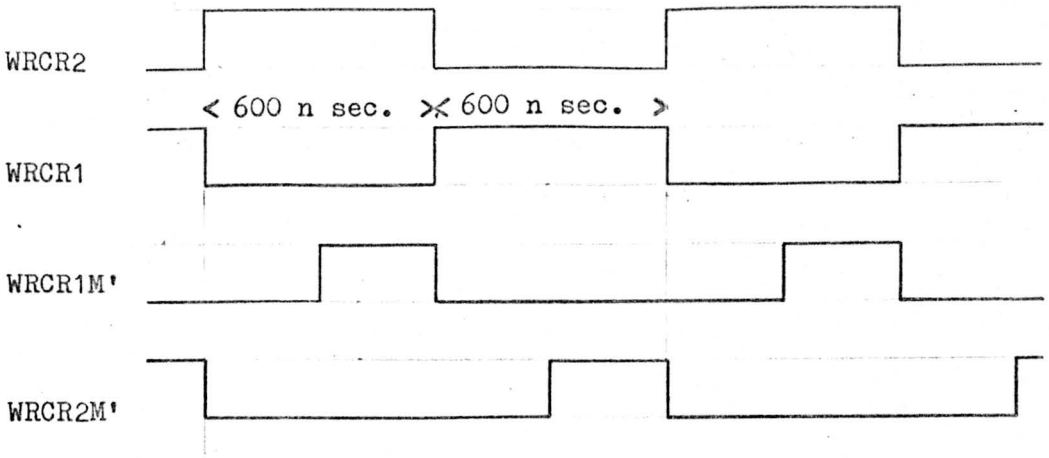


Fig. 14

In a similar way but without the safety delay the current sensing signal ERCRM' is derived with TS 19 and TS 20.

4.2.4 SELECTION SECTION

The remaining D-flip-flop in IC1 is used for head selection. On the appearance of TAG 2 the level of the line BUS0 is taken to the output of the flip-flop. The Q-output presents the signal UH * (upper head). As UH * $\hat{=}$ "1" the upper head is selected. The selection flip-flop can also be activated by the signal LHF from the XMX 1408 - testmodule.

4.3 READ PREAMPLIFIER (dwg. no. 5132 199 7110)

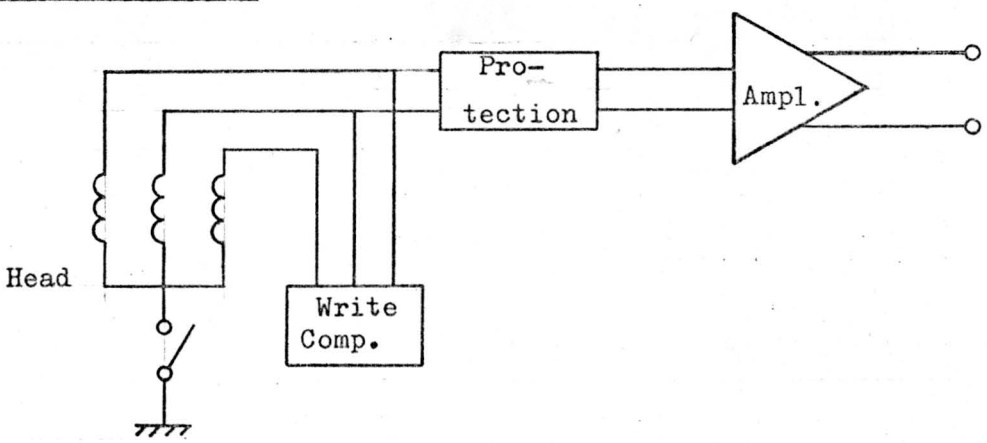


Fig. 15

The read preamplifier contains besides a linear amplifier with a gain of 100 the selection circuits and some components of the write system (Fig. 15). To minimize interference the card is mounted near the heads as close as possible.
The heads are connected to the card with a flexible flatcable.

4.3.1 SELECTION CIRCUITS

The head selection takes place by grounding the common return wire of the desired head coils, for head 1 (upper) with TS 4 and for head 0 (lower) with TS 1.
The signal RDWRK * from the safety circuit on card 07 normally represents a logical "1". As also UH * goes to "1", TS 3 and TS 4 will conduct . The collector voltage

of TS 3 cuts off TS 2 and TS 1 via R 20, so head 1 is selected. As soon as UH * goes to "0" TS 3 and TS 4 cut off and TS 1 and TS 2 start to conduct via R20, so head 0 is selected. In an unsafe condition RDWRK * will represent "0" and TS 2 and TS 3 are both cut off independent of the level of UH *, both heads are disconnected.

4.3.2 WRITE-ERASE-COMPONENTS

To get small risetimes of the write current, in spite of the large capacity of a long wire connection between write amplifier and heads, the current determining resistors R2 to R7 are housed close to the heads on card 13. With the low output inpedance of the write amplifier the wiring capacity will be fast loaded.
Because these precautions are not needed for the erase current only a part of the resistance (R1) is housed on this card.
The diodes GR1 to GR6 form a selection matrix to prevent false currents from flowing through the nonselected head.

4.3.3 PROTECTION

During writing large voltage spikes of +24V and -24V appear across the head. The diodes GR10 to GR21 protect the integrated amplifier from destruction. When reading the diodes GR10-11-18-19 and the diodes of the selected head are kept in conductance by a small (5 mA) current.
C1 and C2 prevent dc-voltages from reaching the amplifier.
With R14-15 and L1-2 besides a correct input impedance a short restoration time is realised.

4.3.4 AMPLIFIER

At last the amplification actions comes actually from IC1, an integrated differential amplifier MC 1410 G. The noisevoltage at the output should be within 2 mVpp (over a bandwidth of 1,2 Me/s). The amplitude of the output signal is approximately 150 mVpp single ended for a zero pattern (416,6 Mc/s) See fig. 16

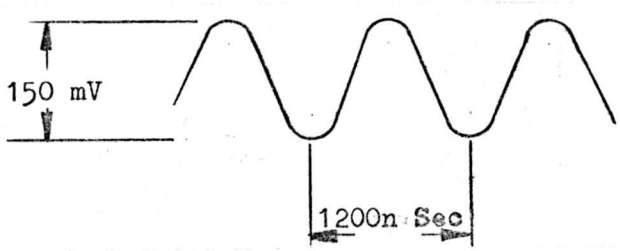


Fig. 16

4.4 READ-AMPL./PHASE CORR. (dwg. no. 5132 198 7110)

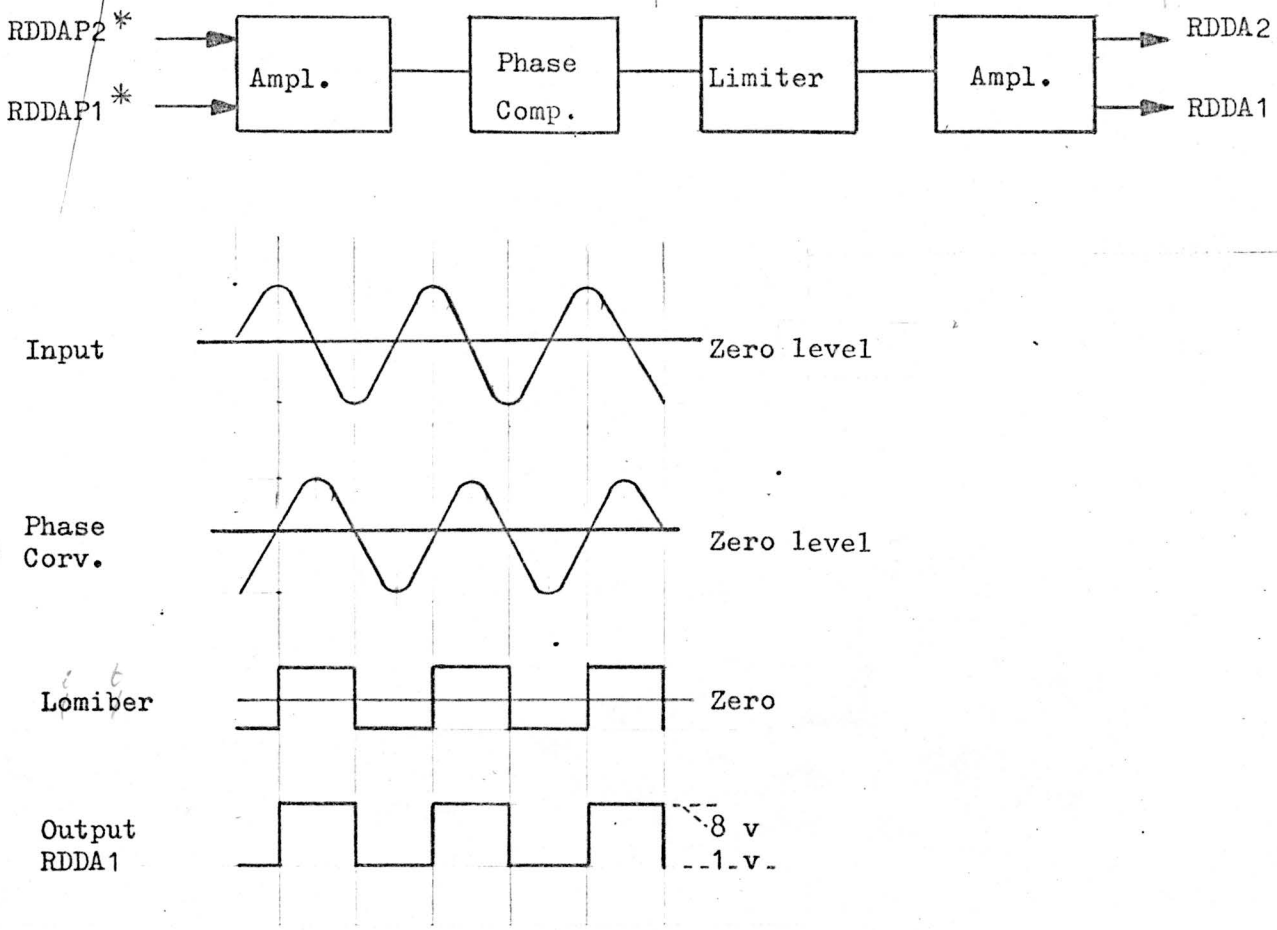


Fig. 17

On card 04 the tops of the input signal are detected by a differentiating process, the tops are transferred in zero crossings. In the limiter section special care has been taken to maintain the zero level. The signal is amplified to a square pulse with steep edges at the zero crossings. (see fig. 17).

4.4.1 THE CIRCUIT

The linear amplifier formed by TS 1 and TS 2 as a long-tailed pair is preceded by a bandwidth limiting circuit R1-C1-R2-C3 and is followed by a double emitter follower TS 3. The RC-circuits C9-R19 and C10-R-18 introduce the 90° phaseshift for peak detection. TS 4 and TS 6 make a two-stage limiter with TS 5 and TS 7 as current sources. Both stages have a high gain with limiting diodes GR3 to GR 6 between the collectors thus preventing saturation of the transistors. With R27 the first stage can be adjusted for correct zero cross detection. (Testpoint AB 19) The output of the limiter is supplied to the last amplifier stage TS 10. TS12 serves as an emitter follower for matching to the next circuit.

4.5 READ RECOVERY (dwg. no. 5132 198 9110)

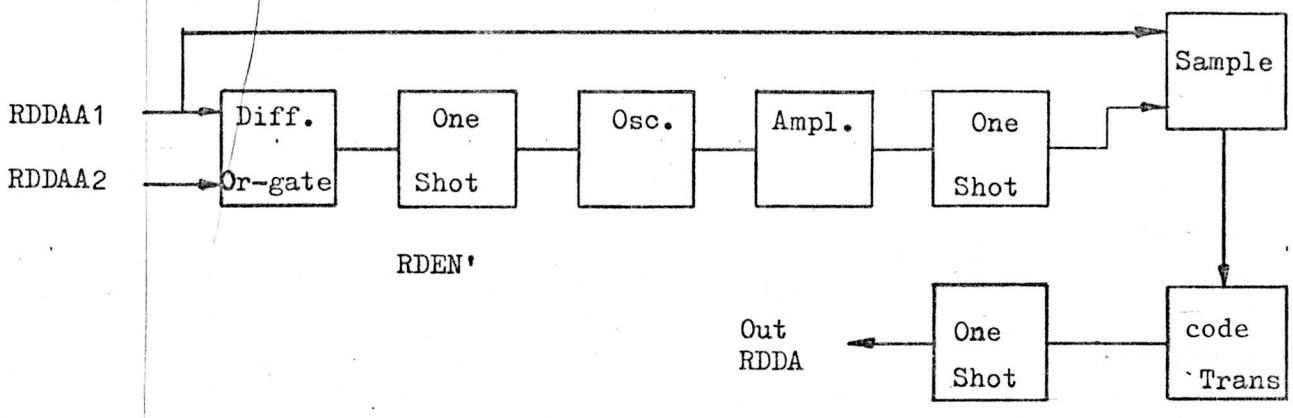


Fig. 18

This part of the system contains the synchronised flywheel oscillator that samples the read signals by means of a D flip-flop.
Also the transfer to the interfacecode takes place on card 05.

4.5.1 RECOVERY (see fig. 19)

The readsignals from card o4 are differentially fed to the input of the read-recovery. The R.C.-elements C_1R_1 and C2 R5 differentiate the square pulses so the pulse edges become spikes the negative spikes are amplified in turn to short pulses. Small differences in TS 1 and TS 2 can be compensated with potmeter R3. With a symmetric signal at the input (duty cycle 50%) R3 is adjusted for equal timedistance between even and odd pulses. (TP1-AB10).
Via emitter follower TS3 a one-shot multivibrator IC1 is started. The output of IC1, in conjunction with GR4-5-6, supplies uniform drivepulses to the flywheel oscillator TS 4. On IC1 there is a possibility to gate the information output with the signal RDEN' (AB 14).
The resonance circuits L1-C8-C9 and L2-C6-C7 are tuned to twice the frequency of an all-one-pattern (1,7 Mc/s).
The sinusoidal output voltage is via the emitter follower TS 5 coupled to the amplifier formed by TS7-9 and current source TS 8. To prevent feedback to the powerline this stage is equipped with the powerstabilization - circuit containing TS 6 and a 8,2V- zenerdiode. For adjustment purposes of L1 and L2 the oscillator signal can be observed at testpoint TP2 (AB 31).
After the emitterfollower TS 10 the signal is clipped with GR9-10-12 to nearly logical levels (-0,7V and +5,4V) and fed to the one-shot-multivibrator IC 5 where one pulse edge is made adjustable with R 36 thus determining the sample moment (TP4- AB27).

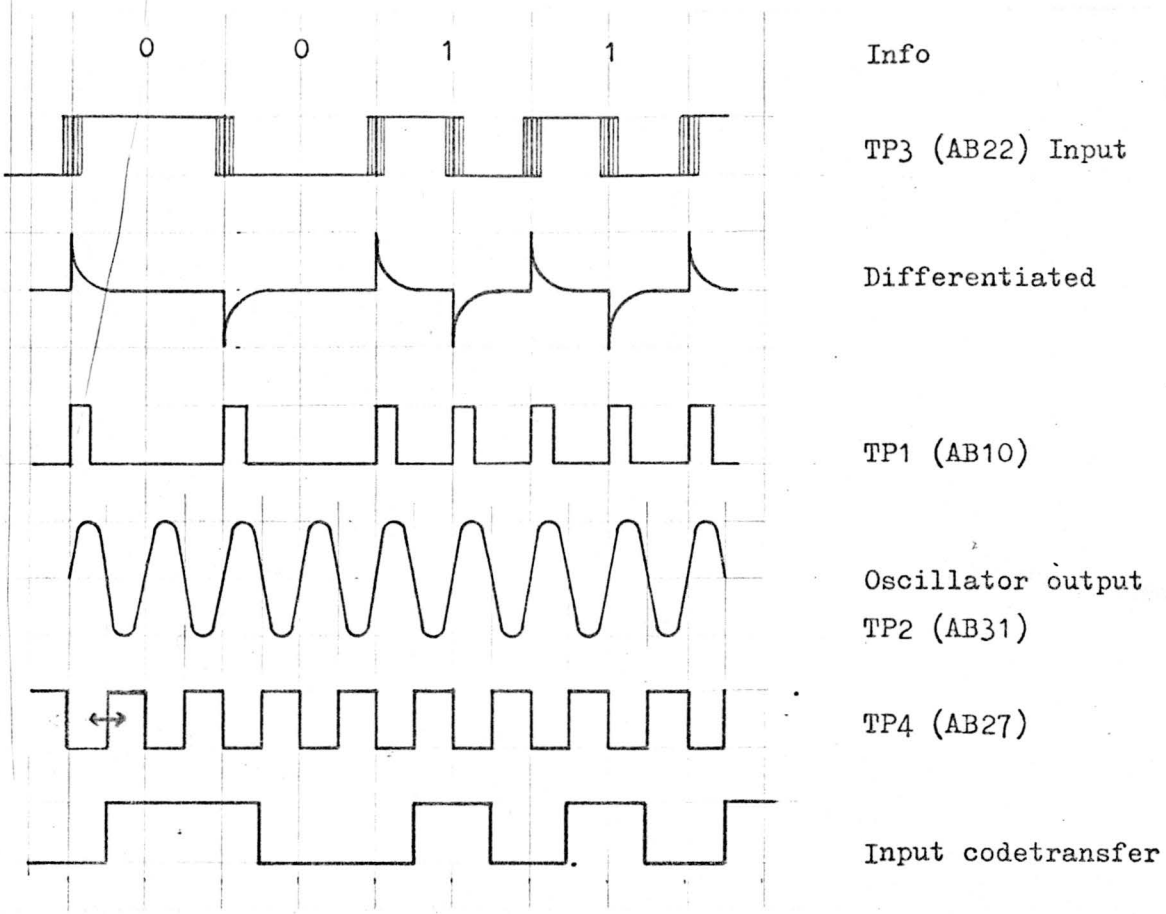


Fig. 19

The input signal RDDAA1 is also clipped to logical levels by emitter follower TS 11 and the diodes GR11-12-13. This signal is brought to the D-input of D-flip-flop IC2. The trigger input T is controlled by the adjustable pulse edge from IC5, so at this edge the information input at D is transferred to the outputs Q as illustrated in fig. 19.

4.5.2 CODE TRANSFORMATION

The interface code expects a pulse with a length of 300 nsec for every pulse edge in the information pattern. This length can be adjusted with R38 on the one-shot multivibrator IC4. The one-shot is triggered with pulse edges derived in turn from IC3 point 3 and IC3 point 6.
After elapse of the propagation delay time, as soon as a pulse appears at the output, the "switch" IC3 is turned over by the outputs Q9 and Q8 of flip-flop IC2, then the system waits for the next pulse edge out of Q5 or Q6 from IC2. The time relation between signals is illustrated in fig. 20.

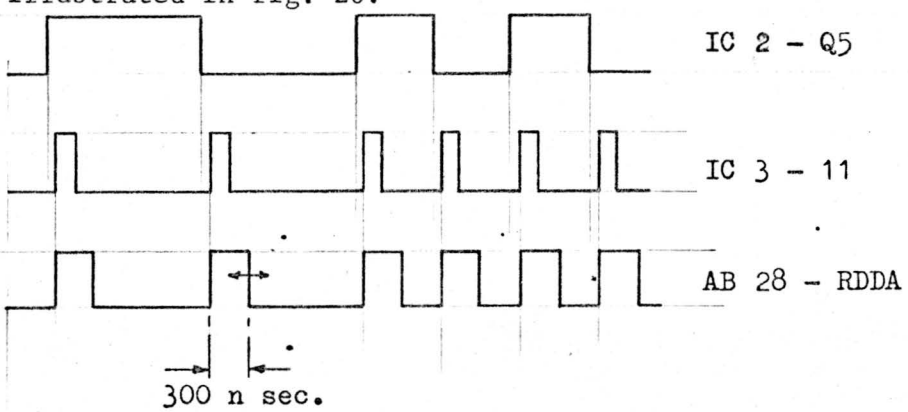


Fig. 20

5. A D J U S T M E N T S

Read - Amplifier/Phase Corr.		Card 04:
Testpoint	TP1 - AB19	
Adjust	R27 for symmetry	
Read recovery		Card 05:
Testpoint	TP1 - AB10	
Adjust	R3 for symmetry	
Testpoint	TP2 - AB31	
Adjust	L1 for max amplitude	
"	L2 for min amplitude	
Testpoint	TP4 - AB27	
	TP3 - AB22	
Adjust	R36 for fig. 21	
Testpoint	AB28	
Adjust	R38 for pulse width = 300 nsec.	

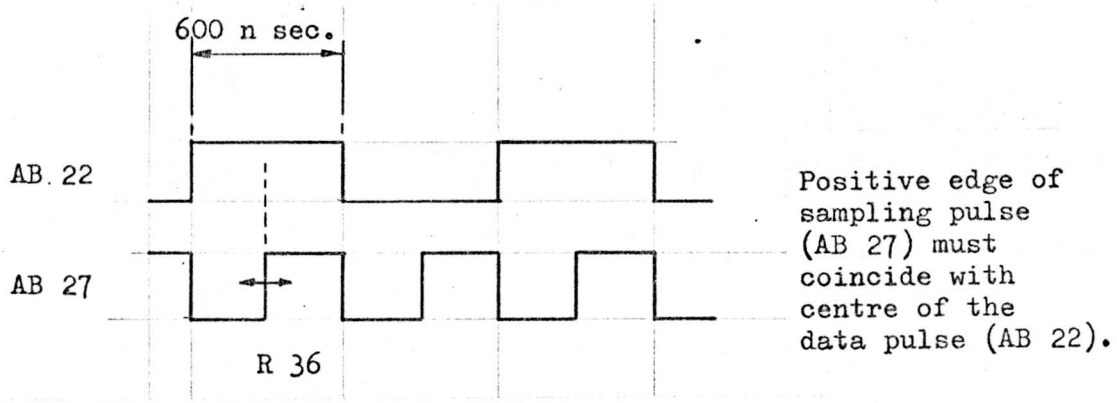


Fig. 21

All cards are factory adjusted and should not need any readjustment during lifetime. Cards are exchangeable without readjustment.

For compatibility the heads in all X1210 units are radial adjusted on track no. 100 with the same radius by means of a "Customer Engineering Cartridge". On the masterdisk two adjacent tracks with the radius of track 100 are written in a way as shown in fig. 22.

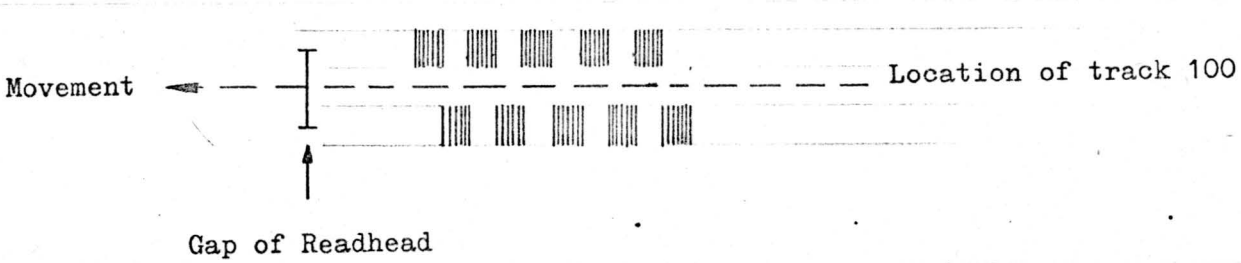


Fig. 22

A correct adjusted head will read from both tracks a voltage with equal amplitude, so no modulation can be observed. (Testpoint 04 AB 4) (See fig. 23a)

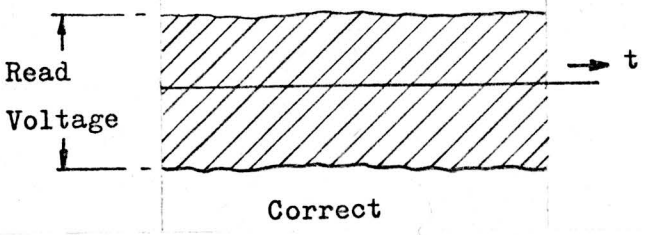


Fig. 23a

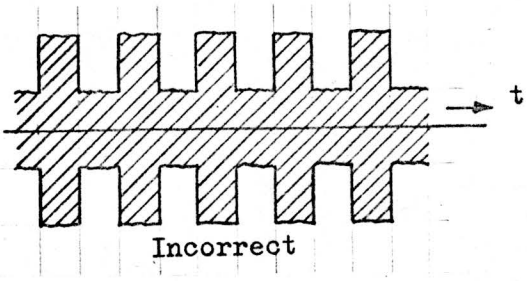


Fig. 23b

As the head adjustment is incorrect the read voltage from one track will differ from the other so an amplitude modulation occurs. (Fig. 23b).
The radial adjustment can be made with a screw located in the headarm mounting construction.

6 POWER SUPPLIES

6.1 POWER SUPPLY UNIT XMX 1407 (dwg. no. 5122 290 9110)

The XMX 1407 is a power supply unit designed specially for the supply of AC - and DC-voltages to the X1210.
The unit contains three Power Supply Modules build together in a 19 inch rack adapter PE 1394. Type PE 1205 is rated for +24V 3,5A max. Type PE 1201 is rated for +5V 3A max. Type PE 1209 is rated for -12V 0,5A max. These modules are amply described in the pamphlets 9499 150 03177/02777/03977 respectively. The incoming main supply is brought to the modules via a noise suppression filter and a panel switch and is passed out for AC-supply of the X 1210. A neon panellamp lights when the unit is switched on.
The +5V supply from PE 1201 is protected for overvoltage with a "crow bar" adjusted at +6V. When the voltage should rise above this value the output is short circuited by a thyristor. The PE 1201 and PE 1205 are adjustable with potmeters attainable behind the front panel of the unit. The adjusting screw of the PE 1209 can be reached from the left side. To compensate for the voltage drop across the cable to the X 1210, the PE 1201 must be adjusted for +5,3V.

6.2 SAFETY/SUPPLY/CLOCK/SPEED (dwg. no. 5132 199 1110)

Because within the X 1210 there is also need for a +12V and a -6V supply on card 07 these voltages are derived from the +24V and -12V respectively. No adjustments can be made on these voltages.

6.2.1 + 12V SUPPLY

A +12V supply is made out of +24V by means of the series resistor R6. The current through R6 and thus the voltage drop is determined by the loading of the circuitry and of the parallel stabilizing circuit formed with TS 1 and TS 2.
Variations in the value of the +12V supply are fully coupled to the bases of TS 1 and TS 2 via the diodes GR 1 and GR 2. The collectors of both transistors draw a compensating current variation through R6 keeping the output voltage almost constant.

6.2.2 -6V SUPPLY

In a similar way as the +12V this voltage is stabilized by a compensating voltage drop across R7. The parallel stabilization takes place via GR 3 and TS 3.

6.2.3

The remaining circuits on card 07 are not applicable to this part of the subject

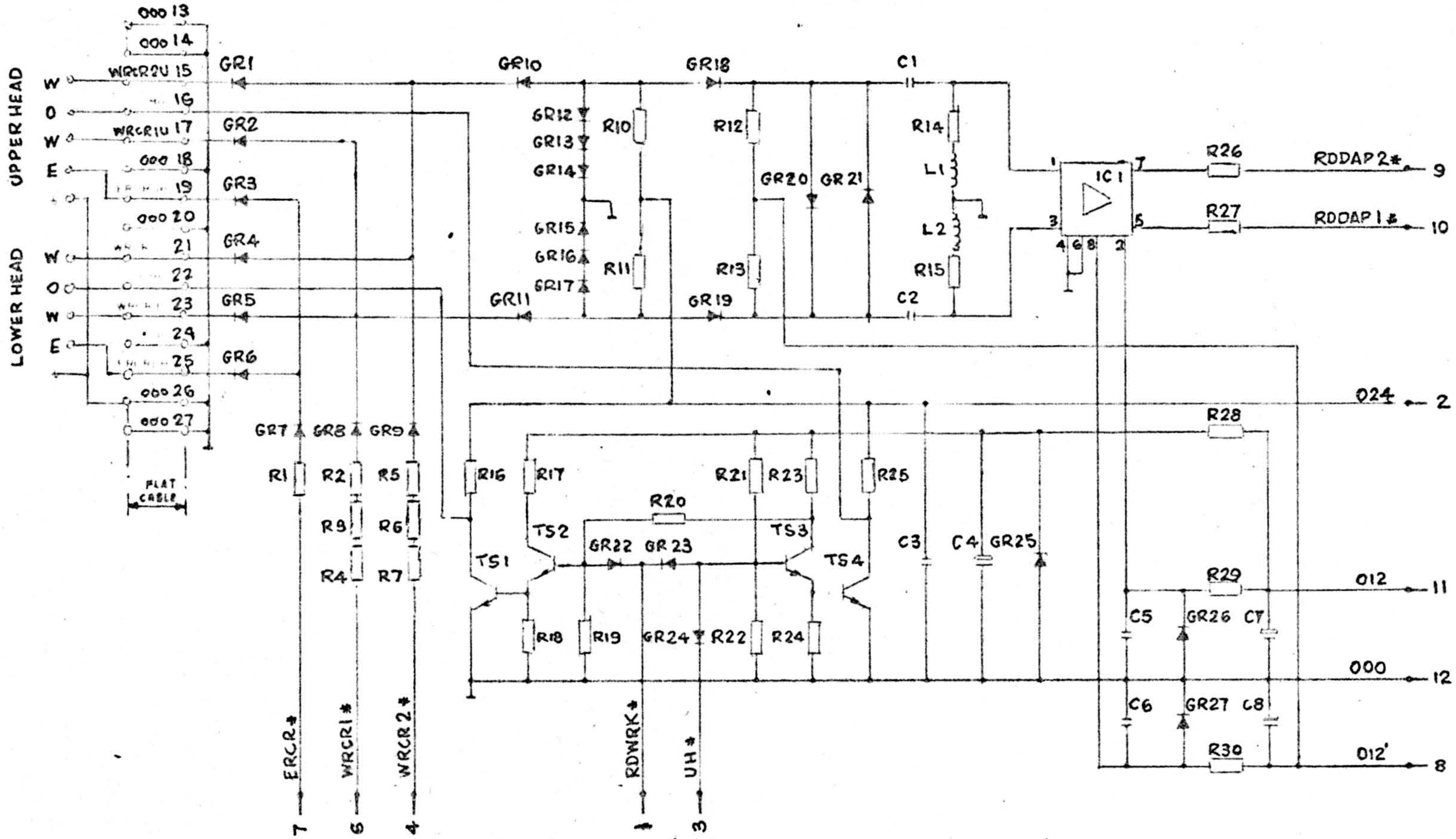
SDU20 - CARD 13

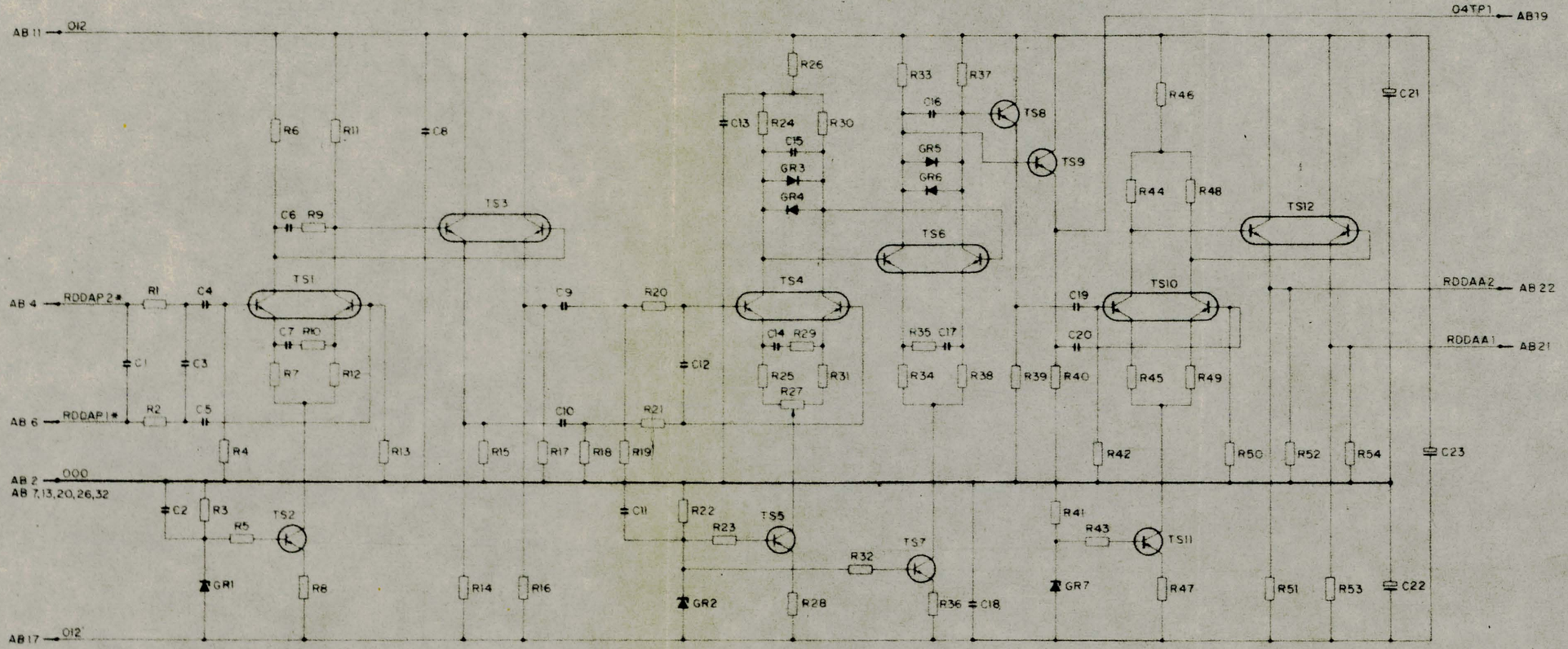
READ - PREAMPLIFIER

5132 199 7110

PHILIPS AG ZÜRICH CH

24.5.71

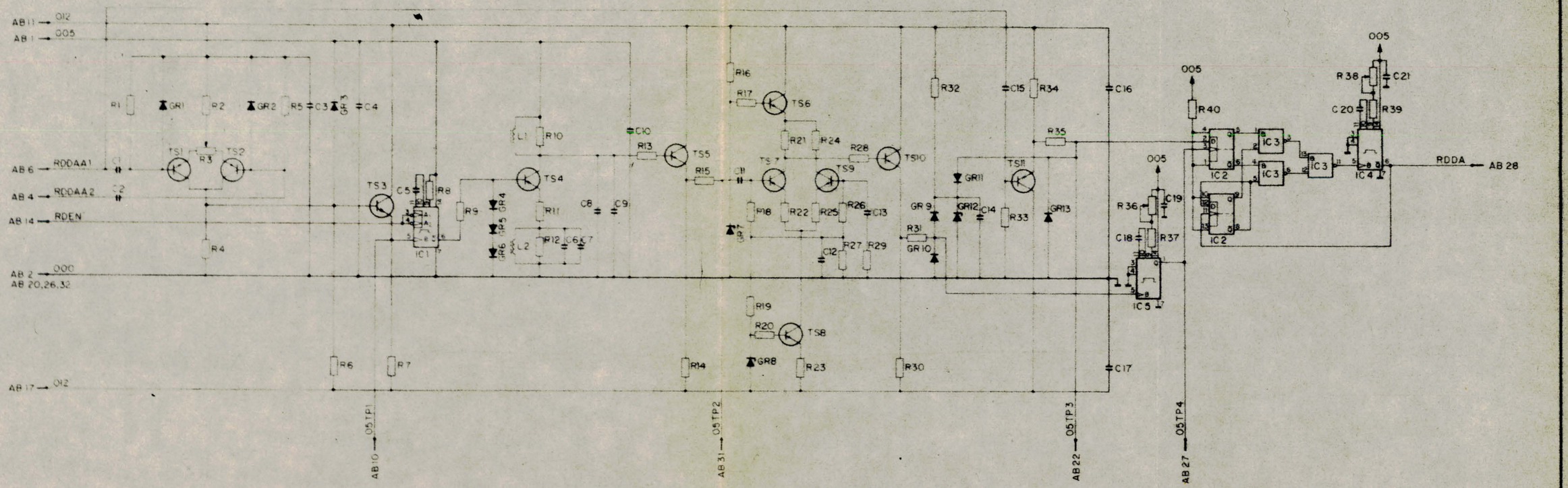




Class No.	SDU20 - CARD 04	12-stellige Ziffercode	12 Ziffer 1
30.4.71 CB	READ-AMPL./PHASE-CORR.	5132 198 7110	
Name	Supers Ersetzt	1 Sh Bl	Bl. 130 – 1
BZ 1	Property of Eigentum von	Check Kontr	Date Datum 8.6.71

Form. A3

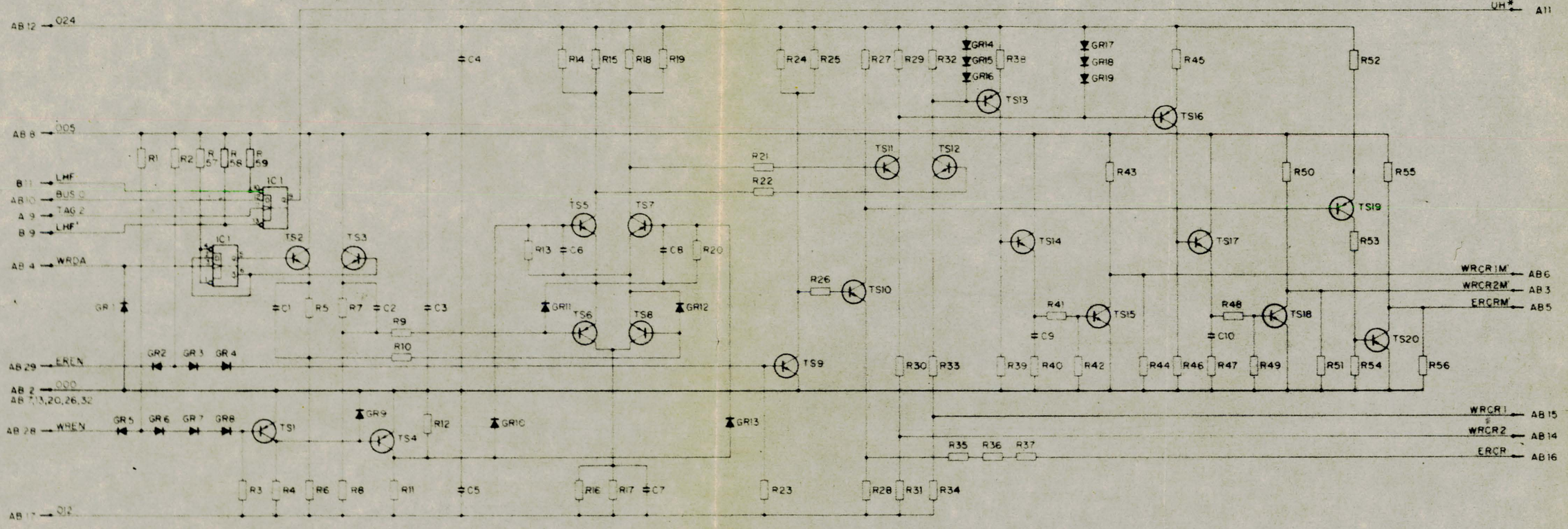
2832 100 00501



Class No	SDU20 - CARD 05	12-stellige Ziffercode	12 Ziffer
30.4.71 CD	READ - RECOVERY	5132 198 9110	1
Name	Supers Ersetzt	1 Sh. Bl.	Sh. Bl. 130 – 1
BZ 1	Property of Eigentum von		Check Kontr. Date Datum 8.6.71

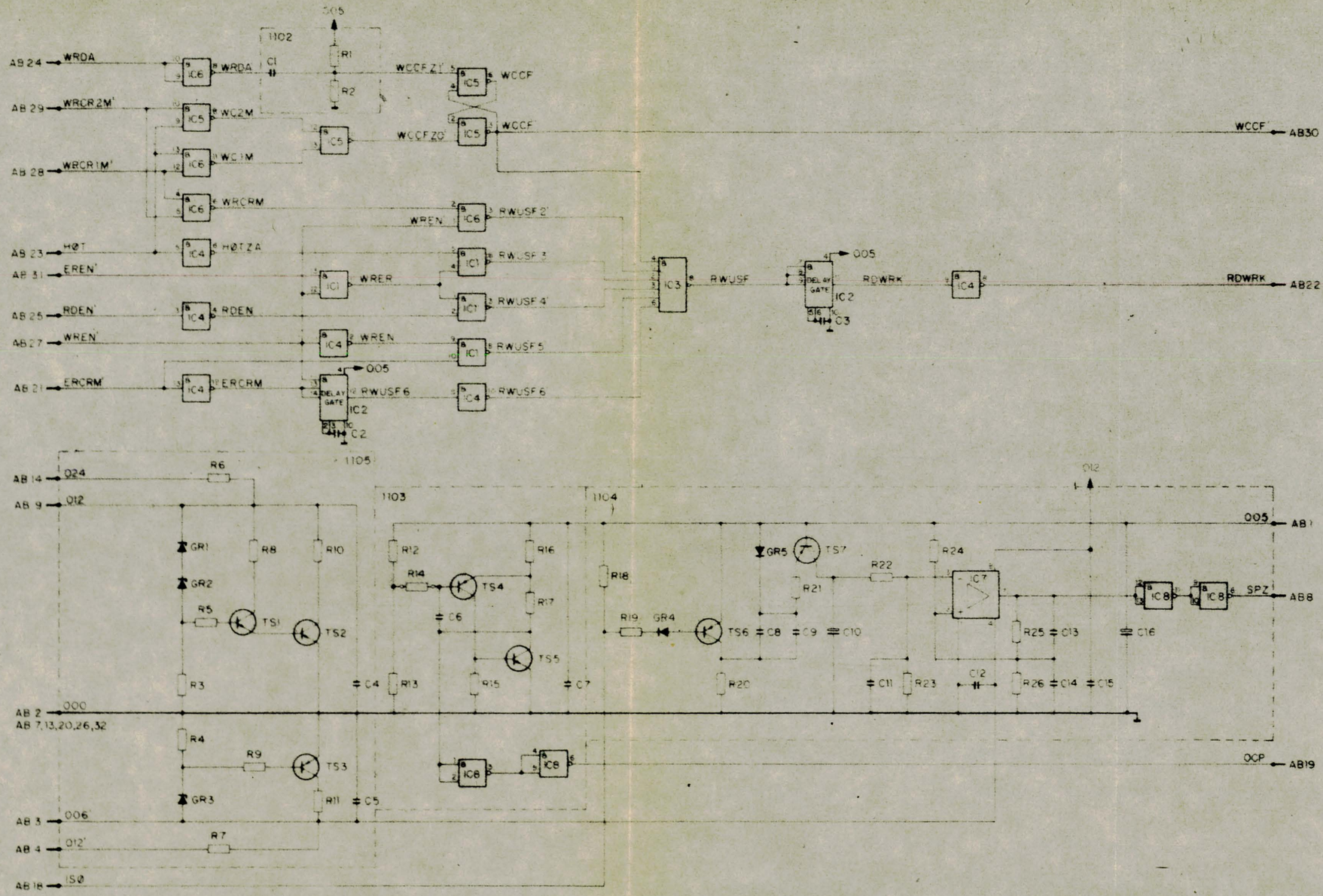
Form. A 3

2832 100 00501



Class No	SDU 20 - CARD 06	12-stellige Ziffercode	12 Ziffer
30.4.71 00	WRITE-ERASE-AMPL. / SAFETY	5132 199 0110	1
Name	Supers Ersatzt	1 Sh Bl	Sh Bl 130 - 1
BZ1	Property of Eigentum von		Check Kontr Date Datum 8.6.71

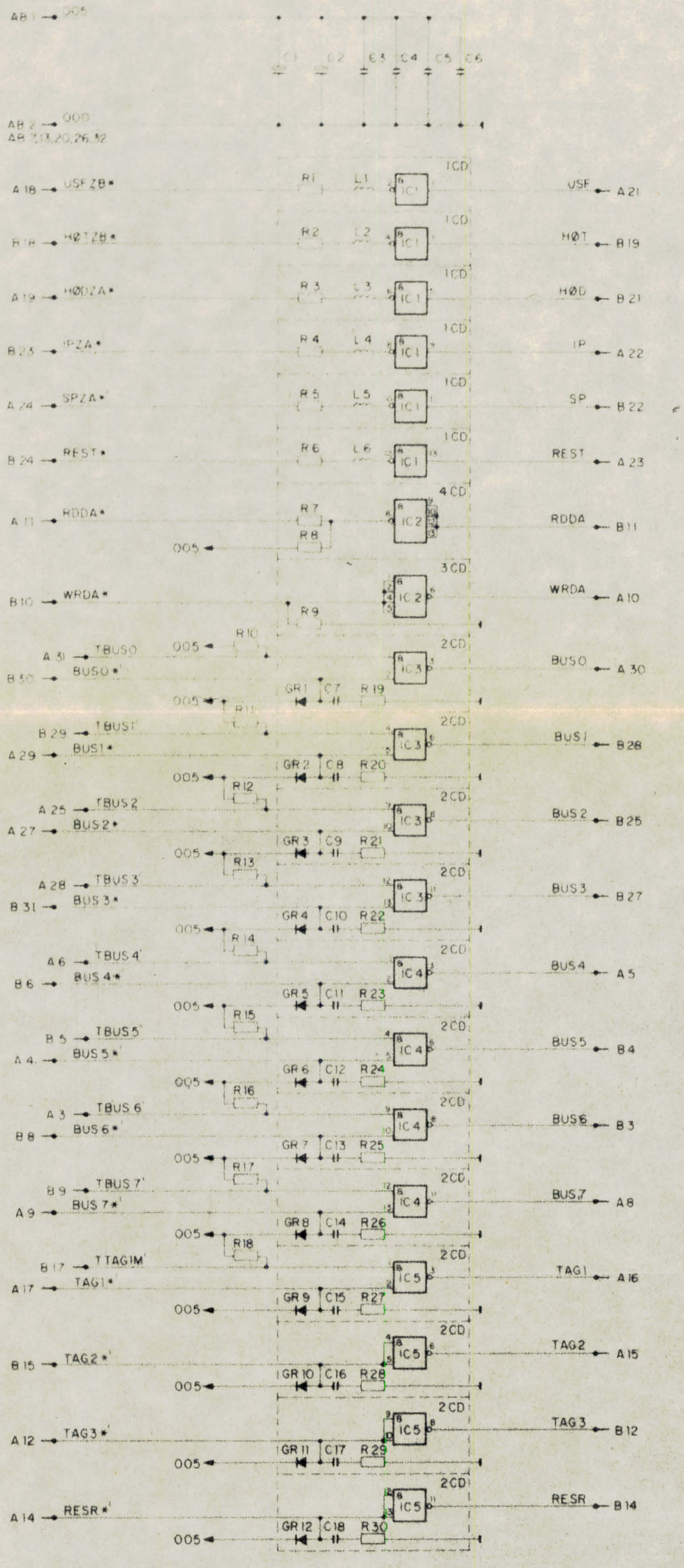
Form A3



Class No		SDU20 - CARD 07	12-stellige Ziffercode / 12 Ziffer: 5132 109 1110 / 1
30.4.71	OB	SAFETY/SUPPLY/CLOCK/SPEED 0	
Name	Supers Ersatzt	1 Sh Bl	Sh Bl 130 - 1
BZ 1	Property of Eigentum von		Check Kontr Date Datum 8.6.71 — Form A 3

2832 100 00501

2832 100 00501



Class No	
Name	30.4.77 CB
BZ1	
Property of / Eigentum von	SDU 20 - CARD 12 TRANSMITTER-RECEIVER
Supers. / Ersetzt	
1 Sh. / Bl.	12-stellige Ziffercode: 5132 199 6110
Sh. / Bl. 130 - 1	12 Ziffer: 1
Check / Kontr	Date / Datum 8.6.77
Form A3	

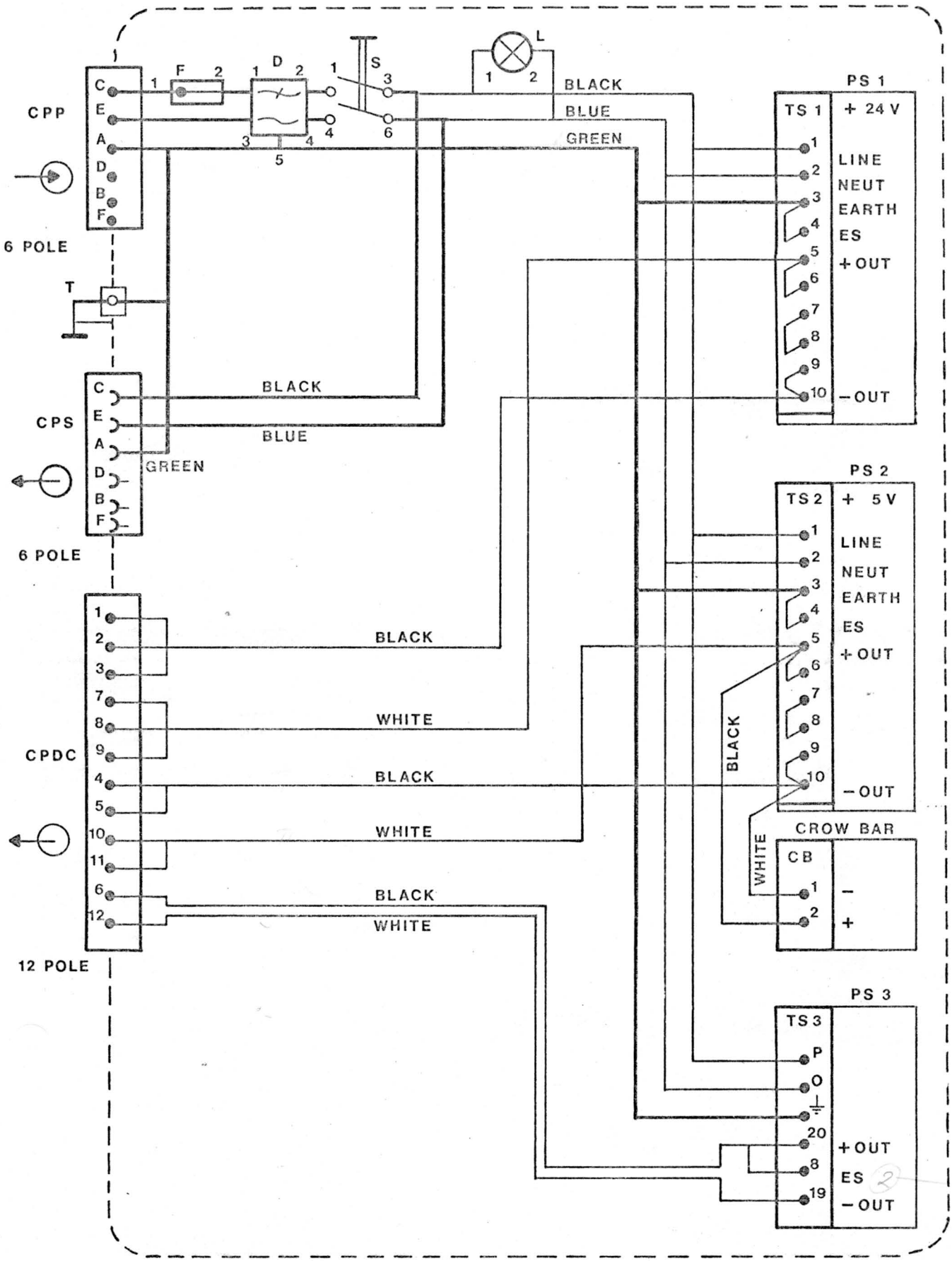


FIGURE 5. XMX 1407 POWER SUPPLY (INTERNAL WIRING)

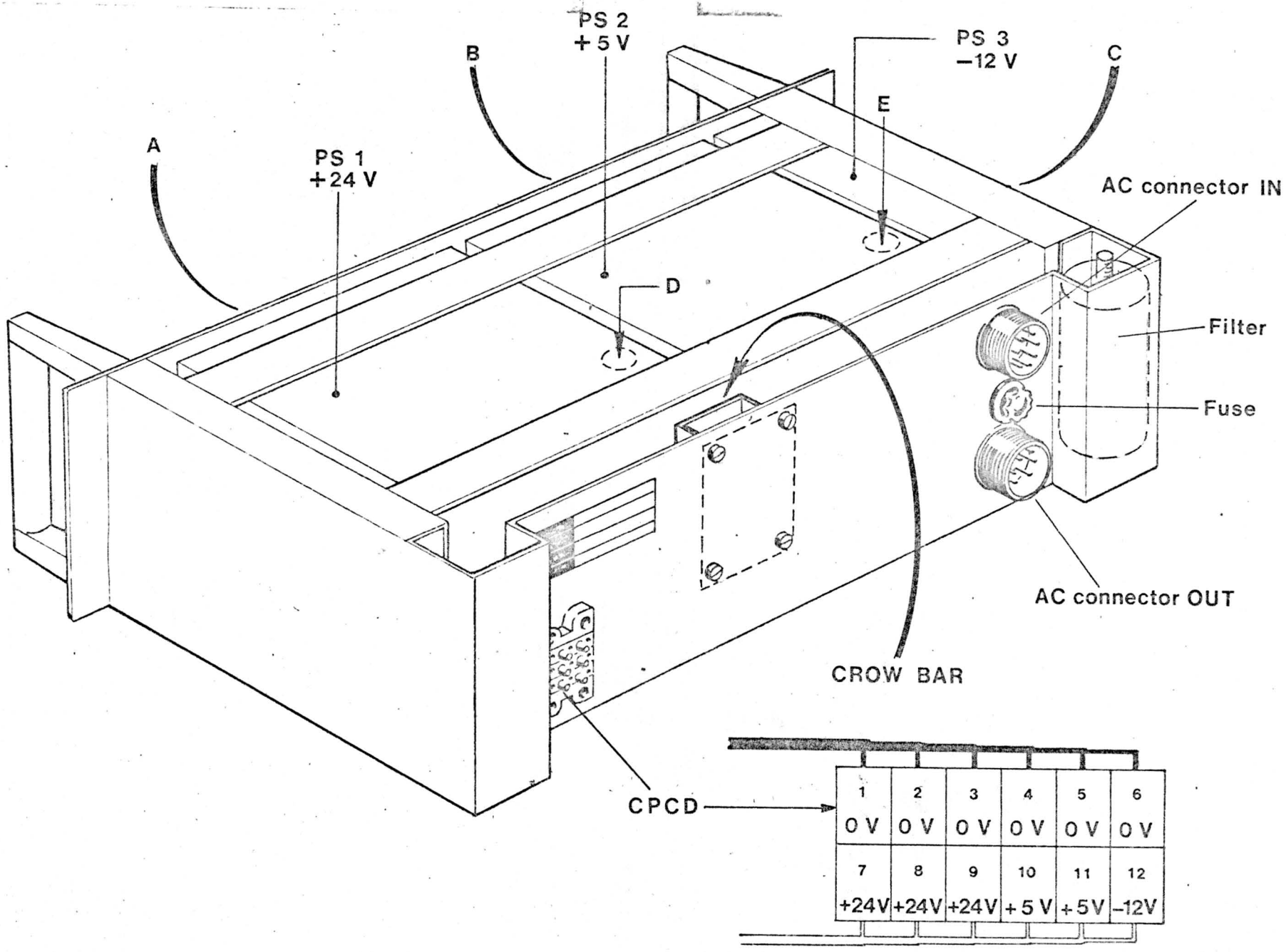


FIGURE 5. XMX 1407 POWER SUPPLY ADJUSTMENTS AND COMPONENT LOCATION